IN THE UNITED STATES DISTRICT COURT

MARSHALL DIVISION

ALACRITECH, INC., Plaintiff, v. CENTURYLINK, INC., *et al.*, Defendants, INTEL CORPORATION, CAVIUM, INC., Intervenors.	Case No. 2:16-cv-693 (LEAD CASE) Case No. 2:16-cv-692 Case No. 2:16-cv-695

DEFENDANTS AND INTERVENORS SECOND ELECTION OF PRIOR ART

Defendants and Intervenors hereby serve its Second Election of Prior Art ("Election") pursuant to the Court's June 7th, 2017 Order (Dkt. 267). This Election relates to the following asserted U.S. patent and claims:

U.S. Patent No. 7,124,205 ("the '205 Patent"), claims 1 and 22;

U.S. Patent No. 7,237,036 ("the '036 Patent"), claims 1, 2, 3, and 4;

U.S. Patent No. 7,337,241 ("the '241 Patent"), claims 1, 9, and 12;

U.S. Patent No. 7,673,072 ("the '072 Patent"), claims 1, 15, 17;

U.S. Patent No. 8,131,880 ("the '880 Patent"), claims 32 and 41;

U.S. Patent No. 8,805,948 ("the '948 Patent"), claims 17 and 22 (collectively "Asserted Patents" and "Asserted Claims").

Defendants and Intervenors explicitly incorporate by reference herein the invalidity contentions (and charts attached thereto) served on Plaintiff on November 11, 2016 by the

Defendants in the above-captioned action(s) ("Defendants' Nov. 11 Invalidity Contentions"), Defendants' supplemental invalidity contentions (and charts attached thereto) served on Plaintiff on January 10, 2017 via email by the Defendants in the above-captioned action(s) ("Defendants' Jan. 10 Invalidity Contentions"), Intervenor Intel's invalidity contentions (and charts attached thereto) served on Plaintiff on February 7, 2017 ("Intel's Feb. 7 Invalidity Contentions), Intervenor Intel's amended invalidity contentions (and charts attached thereto) served on Plaintiff on May 23, 2017 ("Intel's May 23 Invalidity Contentions"), as well as Intervenor Intel's amended invalidity contentions (and charts attached thereto) served on Plaintiff on June 16, 2017 ("Intel's June 16 Invalidity Contentions"), and, subject to this Election, Defendants and Intervenors reserve the right to rely on the invalidity positions presented therein. Finally, to the extent permitted by the Court, Defendants and Intervenors each reserve the right to rely on any invalidity positions presented in any future contentions and/or expert reports served on Plaintiff by any Defendant(s) and/or Intervenor(s) in the above-captioned action(s), as well as the right to rely on any invalidity positions presented in any challenges made to any of the Asserted Patents before the United States Patent and Trademark Office.

PRIOR ART ELECTION

Defendants' and Intervenors' Election of currently known prior art references that anticipates and/or renders obvious the Asserted Patents' Asserted Claims under 35 U.S.C. § 102 and/or § 103 (pre-AIA) expressly or inherently is listed below.

Each of the references and systems listed below qualifies as prior art under one or more sections of 35 U.S.C. §§ 102 and/or 103, as detailed the Defendants' and Intervenor's invalidity contentions to date. The invalidating disclosure in each of the listed references and materials is express, implicit, and/or inherent. Defendants and Intervenors reserve the right to rely on prior

art in Defendants' and Intervenors' productions, prior art produced by Plaintiff or third parties, and/or prior art cited in the Defendants' and Intervenors' invalidity contentions to show the state of the art, and/or the knowledge of a person of skill in the art. The references listed below may also be relied upon to show the state of the art in the relevant time frame. Also, to the extent that any of the references listed below are deemed not to be prior art, they may nevertheless provide evidence of prior or simultaneous invention, thereby supporting the obviousness of the asserted claims.

'205 Patent Elected Art

1. The combination of Intel Prior Art Zero Copy[1] and Satran II[2]
2. The combination of Intel Prior Art Zero Copy and the SMB Technical Standard[3]
3. The combination of Thia[4], Satran I[5], and Satran II
4. The combination of Thia, the SMB Technical Standard, and SMB Protocol[6]

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[1] Intel Prior Art Zero Copy is described in Intel's invalidity contentions. This system is described in at least "Stack Off-Loading – Status and recommendations" dated September 1997 (88801DOC005579-005604); "D102 Design Document" (January 1998) (88801DOC001363-1411); Intel 82550 Product Brief (2001) (Gamla) (88801DOC01547-48); Intel 82550 Specification (May 1999) (Gamla) (88801DOC002853-003064)

[2] J. Satran, Internet Task Force Draft entitled "iSCSI (Internet SCSI)" (June 2000) ("Satran II") (DEFS-ALA0004538-DEFS-ALA0004598)

[3] Technical Standard: Protocols for X/Open PC Interworking: SMB, Version 2 (1992) ("SMB Technical Standard") (DEFS-ALA0003958-DEFSALA0004491)

[4] Y.H. Thia and C.M. Woodside, A Reduced Operation Protocol Engine (ROPE) for a multiple-layer bypass architecture (1995) ("Thia") (DEFS-ALA0010834-DEFSALA0010849)

[5] J. Satran, Internet Task Force Draft entitled "SCSI/TCP (SCSI over TCP) (February 2000) ("Satran I") (DEFS-ALA0004492-DEFS-ALA0004537).

[6] Microsoft Corporation, SMB File Sharing Protocol (January 1, 1996) ("SMB Protocol") (DEFS-ALA0016686- DEFS-ALA0016879)

5. Connery System[7]

'036 Patent Elected Art

1. The combination of Erickson[8] and Tanenbaum[9]
2. Intel Prior Art Zero Copy
3. The combination of Intel Prior Art Zero Copy and Intel Prior Art TSO
4. The combination of Rutsche[10] and Rutsche92[11]
5. Connery System

'241 Patent Elected Art

1. Connery 169[12]

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[7] The term "Connery System" makes reference to the system conceived of by Glenn Connery no later than May 15, 1997. This system is described in at least "Connery Priority Statement" (HPE0007361-7367), "Connery Invention Disclosure" (ALA09262723-2731), U.S. Patent No. 5,937,169 ("Connery 169"), and U.S. Patent No. 6,246,683 ("Connery 683").

[8] As used in Defendants' and Intervenors' invalidity contentions, the terms "Erickson" and "Erickson 618" both make reference to the same piece of prior art: Erickson, U.S. Patent Number 5,768,618 (filed Dec. 21, 1995, issued Jun. 16, 1998) (produced at 88801DOC002764-88801DOC002776).

[9] Andrew S. Tanenbaum, Computer Networks (1996) ("Tanenbaum") (Excerpt at DEFS-ALA0014283-DEFSALA0014320, In full at 88801DOC000050-000882)

[10] Erich Rutsche, The Architecture of a Gb/s Multimedia Protocol Adapter (July 1993) (DEFS-ALA0010789-DEFS-ALA0010849).

[11] Erich Rutsche and Matthias Kaiserswerth, TCP/IP on the Parallel Protocol Engine, High Performance Networking, IV (C-14), IFP Transactions C: Communication Systems, 1992 ("Rutsche 92") (88801DOC001037-88801DOC001059)

[12] As used in Defendants' and Intervenors' invalidity contentions, the terms "Connery 169," "Connery," and "3Com" all make reference to the same piece of prior art: Connery et al., U.S. Patent Number 5,937,169 – Offload of TCP Segmentation to a Smart Adapter (August 10, 1999) (produced at DEFS-ALA0006946-DEFS-ALA0006964)

2. Connery System
3. The combination of Erickson, Tanenbaum, and Alteon[13]
4. The combination of Intel Prior Art Zero Copy and Intel Prior Art Interrupt[14]
5. Intel Prior Art TSO
6. The combination of Rutsche and Stevens II[15]

'072 Patent Elected Art

1. Connery 169
2. Connery System
3. The combination of Erickson and Tanenbaum
4. Intel Prior Art TSO
5. The combination of Kanakia[16], UNDIP[17], and Tanenbaum

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[13] Alteon Networks, Inc., Gigabit Ethernet Technical Brief: Achieving End-to-End Performance (September 1996) ("Alteon") (DEFS-ALA0007016-DEFSALA0007041)

[14] Intel Prior Art Interrupt is described in Intel's invalidity contentions. This reference includes at least Luhmann, U.S. Pat. No 6,195,725 (filed Dec. 14, 1998, issued Feb. 27, 2001) ("Luhmann") (88801DOC006756-00006763); Tim Labatte, Driver Optimization (4/29/97) (88801DOC006451-88801DOC006459); Software Design Document (6/15/1998) (88801D00001363-88801 D00001411); Cordova EAS 82544-EI, 1st Generation, Gigabit Integrated Ethernet MAC/PHY Controller (88801DOC005605-88801DOC005916); GAMLA, External Architecture Specification (EAS) (88801DOC006449, 88801DOC006450); References relating to the Cordova and GAMLA

[15] Gary R. Wright and W. Richard Stevens II, TCP/IP Illustrated Volume 2, The Implementation (February 10, 1995) ("Stevens II")

[16] Hemant Kanakia et al., The VMP Network Adapter Board (NAB): High-Performance Network Communication for Multiprocessors (August 1988) ("Kanakia") (DEFS-ALA0010586-DEFSALA0010600)

[17] Hemant Kanakia et al., Universal Network Device Interface Protocol (UNDIP) (1998) ("UNDIP") (DEFS-ALA0010850-DEFS-ALA0010858)

'880 Patent Elected Art

1. Intel Prior Art Zero Copy
2. The combination of Rutsche and Stevens II
3. The combination of Thia and Tanenbaum
4. Connery System

'948 Patent Elected Art

1. Intel Prior Art Zero Copy
2. The combination of Thia and Tanenbaum
3. The combination of Woodside[18] and Biersack[19]
4. The combination of Woodside, Whetten[20], and Chua[21]
5. Connery System

PRIOR ART SYSTEMS

Defendants' and Intervenors' Election includes prior art systems and uses, which constitute prior art under 35 U.S.C. § 102(a) (known or used in the U.S.), 35 U.S.C. § 102(b) (public use in the U.S.), and/or 35 U.S.C. § 102(g) (made in the U.S.). These prior art systems

[18] C. M. Woodside, K. Ravindran, and R. G. Franks, The Protocol Bypass Concept for High Speed OSI Data Transfer (1991) ("Woodside") (DEFS-ALA0011886-DEFS-ALA0011901)

[19] Ernst W. Biersack, Erich Rutsche, Thomas Unterschutz, Demultiplexing on the ATM Adapter: Experiments with Internet Protocols in User Space (December 1994) ("Biersack") (DEFS-ALA0007066-DEFSALA0007076)

[20] Brain Whetten, Todd Montgomery and Malik Kalfane, A Fast Track Architecture for High Performance, Fault-Tolerant Reliable Distributed Group Communication (February 21, 1995) ("Whetten") (DEFS-ALA0011886-DEFS-ALA0011901)

[21] Roy Chua, MacDonald Jackson, Marylou Orayani, A Fast Track Architecture for UDP/IP and TCP/IP (May 9, 1995) ("Chua") (DEFS-ALA0007163-DEFS-ALA0007180)

and uses include at least Intel Prior Art TSO (*see* Intel's June 16 Invalidity Contentions at pp. 18, 22-26), Intel Prior Art Zero Copy (*see* Intel's June 16 Invalidity Contentions at pp. 18, 26-29), and Intel Prior Art Interrupt (*see* Intel's June 16 Invalidity Contentions at pp. 19, 32-33), which are all detailed in Intel's June 16 Invalidity Contentions. Defendants' and Intervenors' contentions regarding Intel Prior Art TSO, Intel Prior Art Zero Copy, and Intel Prior Art Interrupt are based on their current knowledge and understanding. Defendants and Intervenors expressly reserve the right to amend their invalidity contentions with respect to prior art products and uses upon learning of additional relevant facts, including through third-party discovery.

RESERVATION AND SCOPE

This Election reflects Defendants' and Intervenors' present knowledge and contentions, and, to the extent permitted by the Court, Defendants and Intervenors reserve all rights to modify and supplement this Election without prejudice in the event that additional invalidity or unenforceability grounds are identified. This Election is not, and should not been seen as, admissions or adoptions as to any particular claim scope or construction, or as any admission that any particular element is met in any particular way. Defendants and Intervenors object to any attempt to imply claim constructions from any identification or description of potential prior art. In addition, this Election may rely upon Alacritech's improper assertions of infringement and improper applications of the claims, but Defendants and Intervenors do not agree with those applications and denies infringement.

Defendants and Intervenors further reserve all rights to seek leave to amend this Election in view of, without limitation: (1) information provided by Alacritech concerning its infringement allegations, theories, contentions, facts supporting them, prior suits involving the Asserted Patents or related patents, and/or positions that Alacritech or its fact or expert

witness(es) may take concerning claim construction, infringement, and/or invalidity issues; (2) information provided by Alacritech concerning the alleged priority, conception, and reduction to practice dates for any of the asserted claims; (3) any change by Alacritech in the asserted claims; (4) the claim construction process; (5) additional prior art, including, without limitation, prior art obtained through discovery from Alacritech or a third party, from prior suits involving the Asserted Patents or related patents or challenges to the Asserted Patents in the U.S. Patent Office; (6) amended infringement contentions; (7) an order granting any Defendant or Intervenor leave to amend its invalidity contentions; (8) Alacritech's reliance on grounds not disclosed in its response to Common Interrogatory No. 9 to dispute the invalidity of the references and/or combinations listed above; or (8) any other basis in law or in fact.

Dated: October 20, 2017

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the above and foregoing document has been served on October 20, 2017 to all counsel of record who are deemed to have consented to electronic service via the Court's CM/ECF system per Local Rule CV-5(a)(3).

/s/ Sean Mills